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Practical Implementation of Digital Down Conversion for Wideband Direction Finder on FPGA

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Modern direction finders are designed as sensors for interception of radio signals in wider instantaneous bandwidth. Software radio technology offers ability to develop wideband direction finder architectures with programmable intermediate frequency, instantaneous bandwidth and frequency resolution. In this paper implementation of synchronous digital down conversions (DDCs) for wideband direction finder on FPGA is presented. DDCs are used to downconvert signal from intermediate frequency (IF) to baseband. For wider bandwidth DDCs need to be implemented on FPGA which combines the flexibility of a general-purpose DSP plus the speed, density, and low cost of an application-specific integrated circuit (ASIC) implementation. Measurements and computation of input signals from five channels in parallel on two FPGA devices is presented. Benefits of high speed parallel computing have been observed and discussed in this work. System performance and measured results are briefly presented in paper.

Key words: **direction finder, wide bandwidth, programmable device, signal conversion.**

Introduction

THE determination of emitter positions (emitter geo-locations) has various applications in both civil and defense oriented fields. In the defense applications, the determination of emitter positions is very important in EW (Electronic Warfare) systems and systems for gathering intelligence data such as the COMINT (Communication Intelligence) system. Electronic support (ES), as a part of EW, provides near-real-time information which can be integrated into the Electronic Order of Battle (EOB) for situational awareness [1]. In order to determine emitter position, some of the two-step techniques can be implemented in modern direction finder (DF) system. Two-step positioning techniques, or indirect methods, are based on the estimation of a specified parameter such as the direction of arrival (DOA) or the time of arrival (TOA) at each sensor. The estimated parameters are sent to the central sensor (Fusion Center) in order to determine the emitter location. DOA estimation is usually studied as a part of the more general field of array processing. Many papers in this field are focused on radio direction finding that is estimating the direction of electromagnetic waves impinging on one or more antennas. Modern DFs are based on interception of radio signals in instantaneous bandwidth that is considerably wider than bandwidth of the signals. Instantaneous bandwidth at modern DF is larger than 10MHz. For example, in R&S®DDF0xA Digital HF/VHF/UHF Search Direction Finder instantaneous bandwidth is 10MHz [2] or from 10 up to 40MHz in *mrd5000* and *mrd7000* family of Wideband DF systems (WDF) [3].

In this work we present practical implementation of the one part of the modern direction finder based on the technology of software defined radio using field programmable gate array (FPGA). FPGA technology enables high-speed processing in a compact footprint, while retaining the flexibility and programmability of software radio technology. FPGAs are popular for high-speed, compute-intensive, reconfigurable applications (fast Fourier transform (FFT), finite impulse response (FIR) and other multiply-accumulate operations) [4].

In this paper, we present practical implementation of synchronous digital down conversions (DDCs), from intermediate frequency (IF) to baseband, in WDF with 20MHz instantaneous bandwidth. This DDC is implemented in NI PXI 7975R module (containing DSP-focused Xilinx Kintex-7 FPGA device) extended with NI 5734 adapter module for 4 channel simultaneous 120MHz A/D conversion. This work is a part of research and development of wideband direction finder system for VHF/UHF band in Military Technical Institute from Belgrade, Republic of Serbia.

NI PXIe 7975R [5] is FPGA module for National Instruments PXI platform[6]. PXI platform consists of chassis containing controller and modules.Some of the features of NI PXI Chassis are high-speed lines for direct memory access (DMA) of real-time data (up to 8 GB/s) and user configurable high precision trigger and clock lines. In this application two NI PXIe 7975R modules with NI 5734 A/D converter modules [7] in same PXI chassis are used for signal acquisition and processing.

This paper consists of five parts. Brief introduction is given in Section I, concept of modern DF in Section II, architecture of DDC in Section III, some results of its practical implementations on FPGA are presented in Section IV, and, finally, results and conclusions are given in Section V.

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Concept of modern direction finder

Architecture of a modern WDF consists of DF's antenna array, acquisition channels and digital signal processing block. The basic architecture of modern WDF is presented in Fig.1 [2].

The main role of the antenna array is to perform spatial sampling of the signal of interest (from electromagnetic environment) and to convert spatial electromagnetic wave to guided electric wave (electric current). Acquisition channel includes RF frontend with coherent tuners that convert RF signal to appropriate IF, A/D convertors and digital down convertors (DDC), which convert signal to the baseband. RF frontend consists of antenna multiplexer matrix, low-noise amplifiers and band pass filters. Usually, the signal acquisition in DF may be performed using parallel or sequential techniques. If it is parallel signal acquisition, the measurement of DOA is nearly instantaneous and implements as many signal acquisition channels as signals generated from antenna elements in DF antenna array. In the case of sequential signal acquisition, the number of acquisition channels is lower than the number of antenna elements in DF antenna array. The measurement of DOA is available only after the end of a sequence that involves RF switching, either on the antennas or after phase and/or amplitude weighting of signal from DF antenna array. The basic advantage of sequential signal acquisition is reduced receiver hardware, which implies reduced complexity, cost, volume and weight. However, there is a time-accuracy tradeoff due to less data being gathered, in comparison with a parallel signal acquisition. In the sequential signal acquisition, total time for signal acquisition depends on the number of antenna subsets.

Modern WDF has to provide very high probability of interception of signals. To fulfill this requirement, it is necessary to increase the instantaneous bandwidth or to decrease time for the data processing (which automatically lead to increasing processing speed and processing power). In order to provide wider instantaneous bandwidth, at each acquisition channel there is possibility to form more than one DDC. Using this approach, it is possible to provide instantaneous bandwidth of WDF that corresponds to the number of DDCs and its output sample rate.

The main purpose of the block for digital signal processing is to estimate DOA for all frequency bins in the selected instantaneous bandwidth. In WDF, DOA estimation is performed similar to DOA estimation of wideband signals. Techniques for wideband DOA estimation can be divided into two main groups: coherent and non-coherent [8], according to how information from the covariance matrices are used. The idea of trivial non-coherent DOA estimation of wideband signals is based on non-coherent wideband processing. The non-coherent approach processes each frequency bin independently and averages the DOA estimates over the all bins. Since each decomposed signal is approximated as a narrowband signal, any narrowband DOA estimation method is applicable.

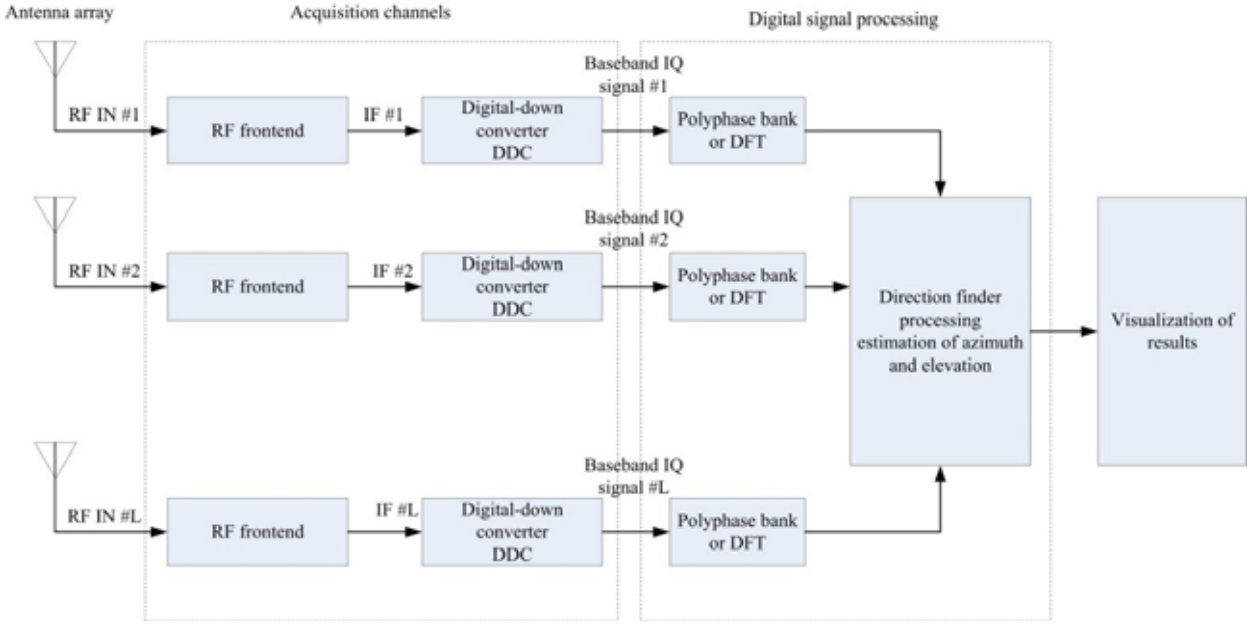

Figure 1. Basic architecture of wideband direction finder

In real-world applications, especially in military systems, non-coherent focusing is most commonly used for the following reasons [8]: no a priori information is required, almost all of the signals are already separated in spectral terms and even with densely occupied scenarios, the signals can be separated in most cases with simple single-wave algorithms and decide the DOA, frequency ranges occupied by the emitters can be estimated.

Usually block for digital signal processing consists of digital filter bank that converts the signal from time domain into the frequency domain (i.e. its frequency spectrum) and part for estimation of DOA. After digital down-conversion to the baseband, the real and imaginary parts of the signal in each measurement path are fed to a digital filter bank, which is conventionally implemented as a Discrete Fourier Transform (DFT) or polyphase filter bank (PFB). During the next processing step, a quantity of samples determined, based on the selected averaging time, is collected and fed to the DOA algorithms. This part of the processing typically involves the use of field programmable gate arrays (FPGAs) or digital signal processor (DSP), because of the necessary high processing speed of the large data and the tight coupling with hardware. The necessary processing power primarily depends from the chosen methods for DOA estimation (Watson-Watt, correlative interferometers, high-resolution methods).

Last part of modern DF system is block for interaction with operator (user) which performs visualization of results from digital signal processing block. This block is software implemented only, commonly referred as GUI (Graphical User Interface).

Architecture of DDC

In telecommunication and SIGINT systems, DDC performs digital mixing (down conversion) of the input signal, narrow band low-pass filtering with decimation and gain adjustment of the digital input stream. It is an essential component of any software radio-based system, which enables simplification of RF front-end design, including local oscillators and mixer design, as the downconversion process is performed in digital domain. Digital filters following the digital mixers provide much sharper filtering than traditional analog filtering. These filters are usually decimating by nature, thereby reduce the output data rate.

Each DDC typically contains an I/Q splitter that is based on a numerical controlled oscillator (NCO) that modulates the input signal that comes from the RF section with sine and cosine waves digital signal generator (mixer to quadrature downconvert the signal to baseband),followed by a multi-stage cascade-integrate comb (CIC) filter (also called Hogenauer filter),and two stages of decimate-by-two filtering to isolate the desired signal: Compensation FIR (CFIR)filter, and a Programmable FIR (PFIR) filter. Simple block-diagram of one DDC is shown on Fig.2 [9].

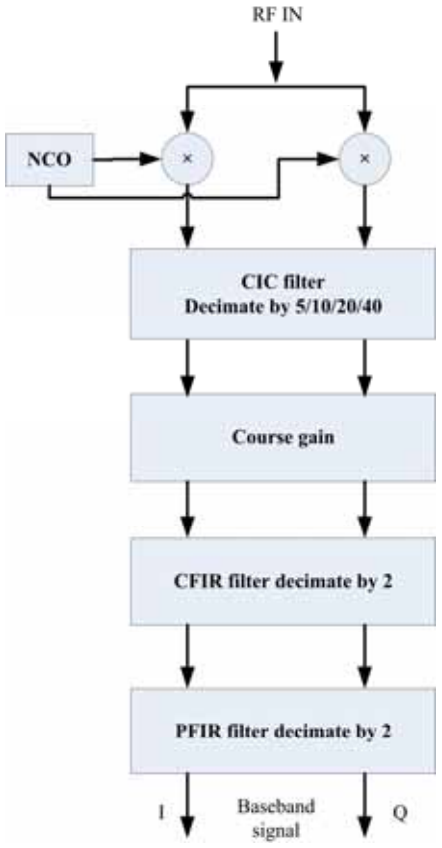

Figure 2. Typical DDC architecture

NCO represent Sine/Cosine signal generator with phase offset and frequency tuning inputs. A positive tuning frequency is used to downconvert the signal, but negative tuning frequency can be used to upconvert the negative (spectrally flipped) image of the desired signal. In the case for demand of full coherent acquisition channels (when DF systems use DOA algorithms with phase estimation), NCO of every DDCs in all channels must be mutually synchronized (in time and frequency). The complexity of the NCO will depend on the final frequency setting accuracy required and on the spurious-free dynamic range (SFDR) of the system.

CIC filter is useful to realize large sample rate changes in digital systems without the need for multipliers and using a very compact architecture (mixer outputs are decimated by large integer factor). It reduces the input signal sample rate by a programmable factor. CIC filter is built using two basic blocks: an integrator and a comb. An integrator is a single pole IIR filter which essentially has a low pass filter characteristic. A comb is a FIR filter. A typical CIC filter is built as a cascade of multiple integrator and comb sections and a rate changer between the two sections (typical number of these multi-stages is from 3 to 6). This filter can achieve high decimation or interpolation rates without using any multipliers, which makes them very useful for digital systems operating at high rates. The CIC outputs are followed by a coarse gain stage and then followed by two stages of decimate-by-2 filtering. The coarse gain circuit allows the user to boost the gain of weak signals after the input bandwidth of the downconverter has been reduced by the CIC filter.

The CFIR filter represents the first stage decimate-by-two, and it is used to flatten the passband frequency response (adjusts for roll-off of the CIC passband), and its typical specifications is shown on Fig.3 [10].

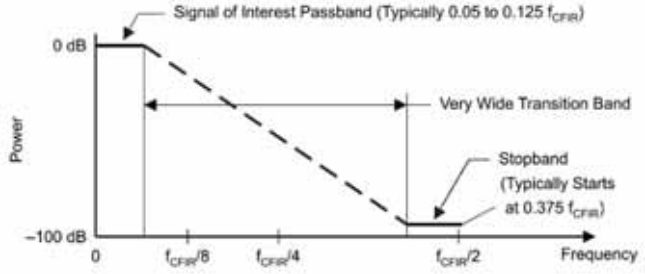

Figure 3. CFIR Specifications

Low-pass PFIR filter is the second decimate-by-two stage and it is used to lower the magnitude of the ripples of the CIC filter and customization of the channel's spectral response. Its typical specifications are shown on Fig.4 [10].A typical use of the PFIR is to perform matched (root-raised cosine) filtering. Outputs from PFIR are complex IQ signals in baseband.

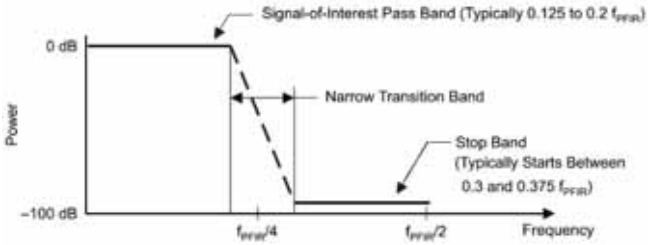

Figure 4. PFIR Specifications

The CIC filter, Compensation FIR, and Programmable FIR blocks are used together in DDC to achieve high decimation ratio, aliasing attenuation and application-specific filtering. Designing decimation filters so that their cascade response meets a given set of passband and stopband attenuation and frequency specifications can be a cumbersome process where we must choose the correct combination of passband and stopband frequencies for each filter stage. Choosing stopband frequencies properly ensures lower order filter designs (stopband attenuation and ripple are controlled by the order of the filters). In the design process, there is a need for relaxing the stopband frequency as much as possible to obtain the lowest filter orders at the cost of allowing some aliasing energy in the transition band of the cascade response. This design tradeoff is convenient in the case of priority, for minimization of the filter orders (to realize it on dedicated hardware platform with limited resources like FPGAs od DSP).

A variety of dedicated DDCs are available, with Analog devices, TI-Graychip (Texas Instruments) and Intersil being the most popular ones today. These DDCs offer programmable bandwidth (or decimation) and tuning frequency. However, they are usually targeted for narrower band applications. There is an increasing demand for higher bandwidth, and system designers are trying to design wideband systems with bandwidths up to 40MHz. These include WDF, radar, GPS, telemetry, wideband communications, etc. For larger bandwidths, the DDCs need to be implemented in a FPGA following the A/D converter.

In the case that required instantaneous bandwidth of the WDF is 20MHz, it can be achieved by combining four DDCs at each acquisition channels with parameters:

- Input sample rate: 120MHz;
- CIC decimation factor: 5;
- CFIR input sample rate:24MHz;
- CFIR decimation factor (fixed): 2;
- PFIR input sample rate:12MHz;
- PFIR decimation factor (fixed): 2;
- PFIR output sample rate:6MHz.

Magnitude responses of CIC, CFIR, PFIR filters and their simultaneous cascade connection, are shown on Pictures 5-8, respectively.

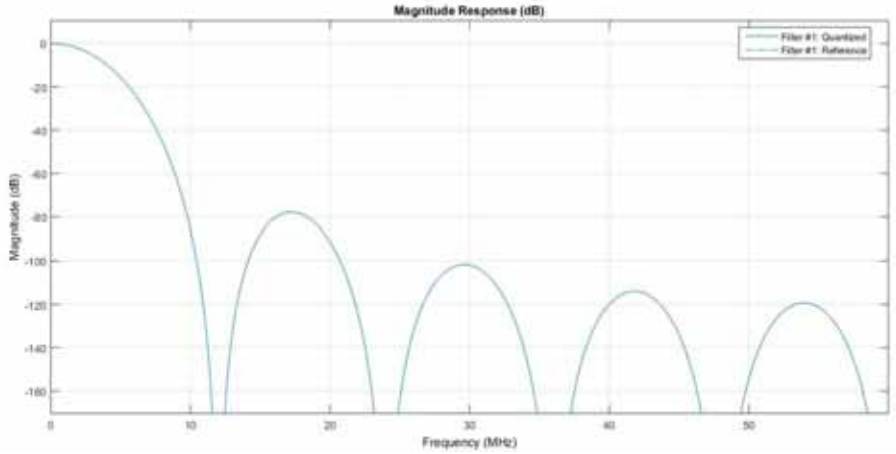

Figure 5. Magnitude response of CIC

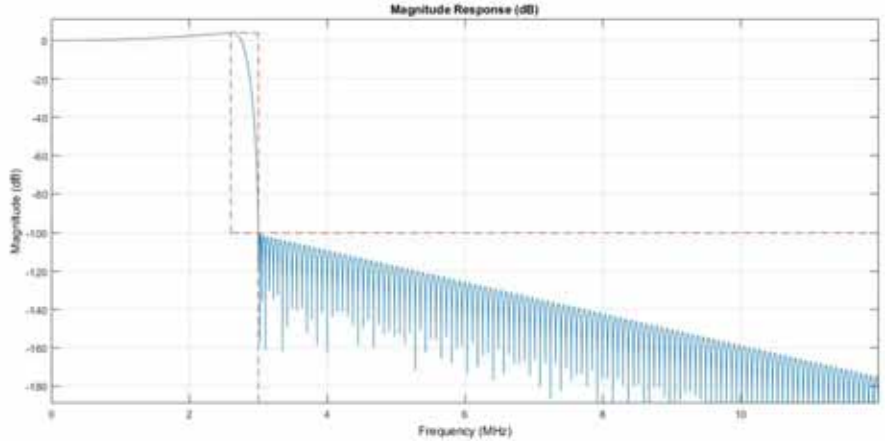

Figure 6. Magnitude response of CFIR

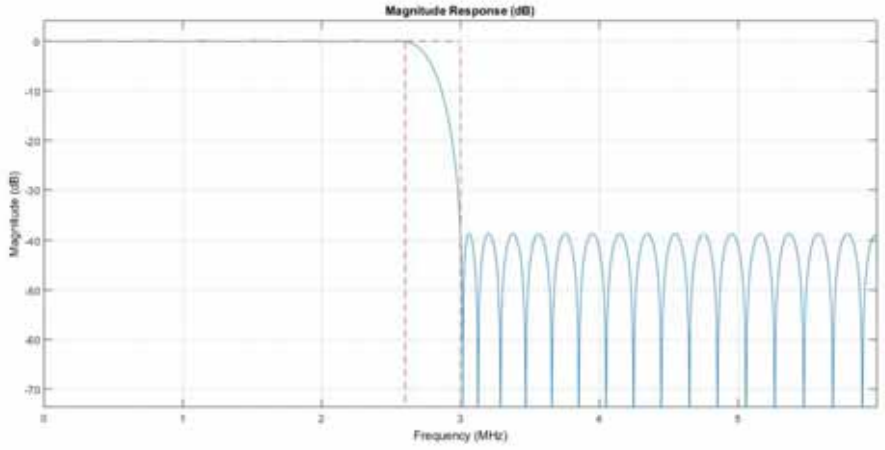

Figure 7. Magnitude response of PFIR

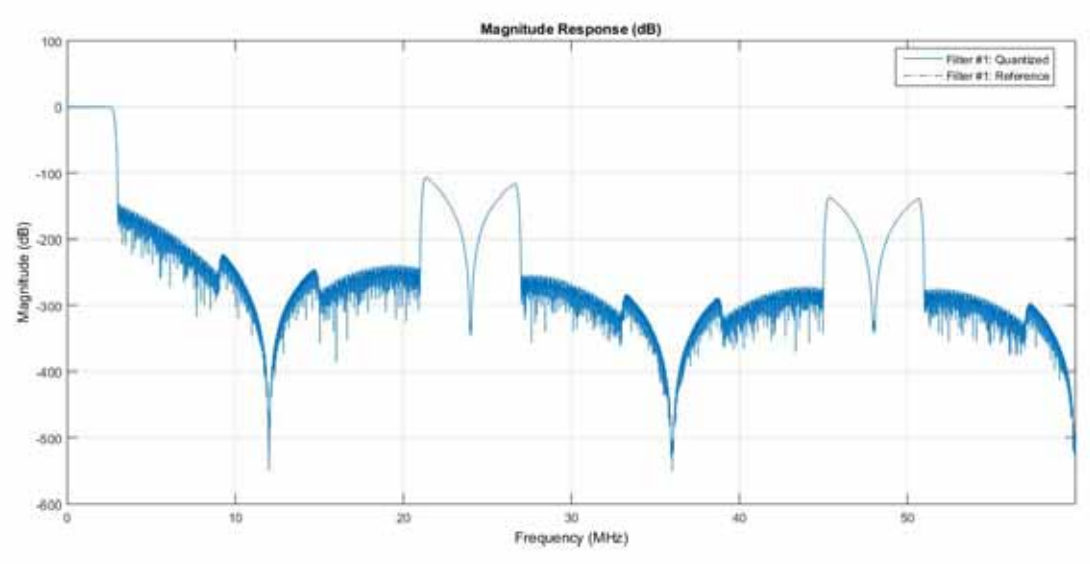

Figure 8. Magnitude responses of cascaded CIC, CFIR and PFIR filters

Implementation on FPGA

Digital down conversion algorithm was implemented using high level programming tools that enabled optimal programming of Kintex-7 FPGA chip on NI PXIe-7975R device. Xilinx IP cores were used for integration of DDC chain elements such as NCO, CIC, CFIR and PFIR filters and LabVIEW FPGA module was used for A/D acquisition, synchronization between 5 channels data transfer, real-time reconfiguration of IP cores.

LabVIEW FPGA module is a graphical programming environment which enables block based FPGA programming. Each block executes arithmetical or logical function. Blocks can be complex structures containing several smaller blocks. Each block has input signals, output signals, synchronization signals for input and output and parameters.

Since processing of some complex blocks can take several sample clock cycles synchronization inputs and outputs are used to signal availability of valid block output. Inputs and outputs can be connected between processing blocks directly or onboard FIFO buffers can be used to transfer data between blocks.

Xilinx IP cores provide optimized and tested DSP blocks. These blocks were configured using parameters obtained in digital filter design of CIC, CFIR and PFIR filters.

Processing was implemented on two NI PXIe-7975R modules in parallel. Three channels are processed on the 1st and the 2nd channel on the 2nd module. Acquisition and processing of all 5 channels had to be synchronous because of implemented DF algorithms. Signal sampling and digital processing were driven by 120MHz sample clock. NI PXI chassis provides 10 MHz reference clock which was used for phase locking (PLL) 120 MHz module sample clocks. Chassis trigger line was used to share start signal for both modules.

After PLL is done and while start trigger occurs in each clock sample, analog input is acquired on all 5 channels as 16bit value. Direct digital synthesizer (DDS) Xilinx core IP is used to generate NCO signal. NCO sine and cosine signals are then multiplied with input sample in mixer block to obtain complex signal (in phase and quadrature phase component signal -I/Q). There are 4 NCO blocks used for down-converting into 4 different sub-bands. Each input signal is mixed with each of 4 NCO signals, which produces 20 complex signals.

Each complex signal is processed in individual DDC chain. Each DDC chain is implemented as individual parallel processing hardware block in FPGA circuit after code compilation. First block in DDC chain is CIC filter implemented as CIC Xilinx IP core block with variable decimation factor. For instantaneous WDF bandwidth of the 20MHz CIC decimation factor is set to 5. Decimation factor can be increased to smaller instantaneous bandwidths. Since CIC filter output signal is significantly attenuated after the decimation , the coarse gain is applied by multiplying complex CIC output signal with gain value. For CFIR and PFIR filter implementation FIR Xilinx IP core block was used. Core was configured to implement filter coefficients previously calculated during digital filter design.

Signals at the output of each DDC chain are transferred to polyphase bank / DFT processing blocks using local FPGA FIFO buffers. FPGA implementation ensures determinism in signal processing due to hardware implementation of processing blocks. Each of 20 DDC complex signal outputs is always sent to FIFO at same clock tick with constant rate of 6MHz.

In FPGA implementation of digital signal processing device, resource utilization is of great importance. Device resource consumption on Xilinx Kintex 7 FPGA is presented for implementation of 12 DDC processing blocks at one I PXIe-7975R module:

- Total slices: 58.3% (37066 out of 63550)
- Slice Registers: 26,6% (135478 out of 508400)
- Slice LUTs: 27,3% (69499 out of 254200)
- Block RAMs: 25,2% (200 out of 795)
- DSP48s: 67,1% (1034 out of 1540)

Functionality and performance of synchronous data processing was verified using CW signal (Figure9) and AM modulated (Pictures 10 and 11) test RF signal with -30dBm power level and 30MHz frequency. Test signal is divided into two signals each on one channel of two different NI 7975R devices in the same NI PXI chassis.

Outputs of corresponding DDC have been compared. Amplitude level differences between two DDC outputs were less than 3% and phase differences were less than 1º for both test signals.

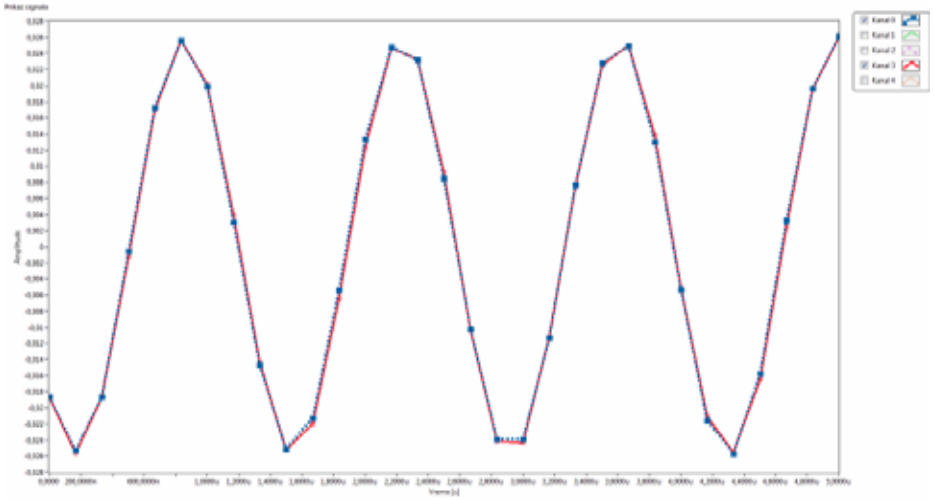

Figure 9. FPGA implemented DDC output - single tone input

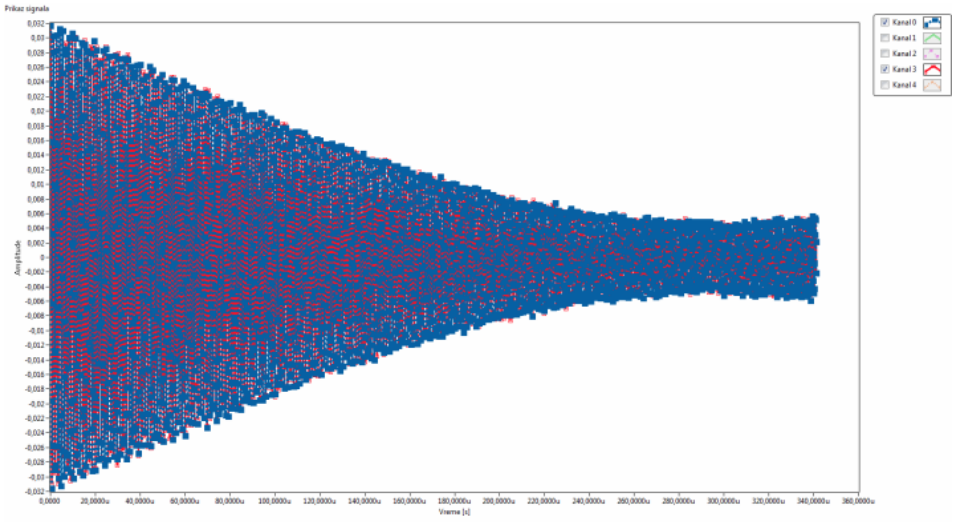

Figure 10. FPGA implemented DDC output -AM modulated input

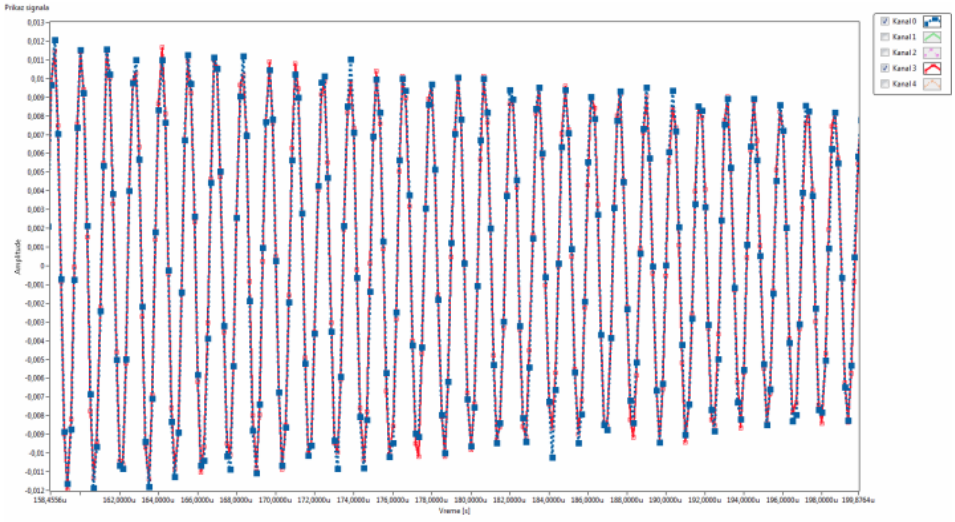

Figure 11. FPGA implemented DDC output -AM modulated input (enlarged)

Conclusions

Modern direction finders are based on interception of radio signals in wider instantaneous bandwidth in order to achieve high probability of interception of the signal of interest. By increasing the instantaneous bandwidth of DF it is possible to improve the probability of interception of the signal of interest. In this paper, we present an approach of increasing the instantaneous bandwidth using combination of four DDCs per each channel of DF. DDCs are implemented in FPGA. FPGAs are becoming an integral part of DF design. FPGA technology enables high-speed processing in a compact footprint, while retaining the flexibility and programmability

of software radio technology. Presented solution could be used in software defined direction finder.

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Praktična implementacija DDC za širokopojasni radio-goniometar na FPGA

Moderni radio-goniometri su dizajnirani kao senzori za presretanje radio signala u širem trenutnom opsegu. Softverska radio tehnologija nudi mogućnost razvoja arhitekture radio-goniometra sa programabilnom među-frekvencijom, trenutnom širinom opsega i frekvencijskom rezolucijom. U ovom radu, predstavljena je implementacija sinhrone DDC za širokopojasni radio-goniometar na FPGA. DDC se koristi za spuštanje signala sa među-frekvencije u osnovni opseg. Za šire opsege, DDC mora biti implementiran na FPGA, kombinujući tako fleksibilnost opšte namene DSP sa velikom brzinom i malom cenom ASIC implementacije. Predstavljena su merenja i proračuni ulaznih signala sa pet kanala u paraleli na dva FPGA uređaja. U radu su posmatrane i diskutovane prednosti velikih brzina paralelnog računanja uz predstavljanje performansi sistema i dobijenih rezultata.

Ključne reči: **radio-goniometar, širokopojasni uređaj, programabilni uređaj, konverzija signala.**

Практическая реализация цифровых понижающих преобразований (DDC - digital down conversion) для широкополосного радиопеленгатора по FPGA

Современные радиопеленгаторы разработаны как датчики для перехвата радиосигналов в более широкой мгновенной полосе пропускания. Программная радиотехника предлагает возможность разработки архитектуры широкополосных радиопеленгаторов с программируемой промежуточной частотой, мгновенной полосой пропускания и частотной резолюцией. В этой статье представлена реализация синхронных цифровых понижающих преобразований (DDC) для широкополосного радиопеленгатора на FPGA. DDC используются для понижающего преобразования сигнала от промежуточной частоты (IF) до основной полосы частот. Для более широких полос пропускания DDC необходимо реализовать на FPGA, который сочетает в себе гибкость общего назначения DSP, а также скорость, плотность и низкую стоимость реализации специализированной интегральной схемы (ASIC). Здесь представлены измерения и вычисления входных сигналов от пяти каналов параллельно на двух устройствах FPGA. В этой работе были рассмотрены и обсуждены преимущества высокоскоростных параллельных вычислений. Производительность системы и измеренные результаты коротко представлены в документе.

Ключевые слова: **радиопеленгатор, широкополосное устройство, программируемое устройство, преобразование сигналов.**

Implémentation pratique de DDC pour le radiogoniomètre large bande sur FPGA

Les radiogoniomètres modernes sont conçus comme les capteurs pour l'interception des signaux radios dans la portée instantanée plus large. Le logiciel pour la radio technologie offre la possibilité de développement de l'architecture de radiogoniométrie à la fréquence intermédiaire programmable, la largeur de portée instantanée et la résolution de fréquence. Dans ce travail on a présenté l'installation de DDC synchrone pour le radiogoniomètre large bande sur FPGA. Le dispositif DDC s'emploi pour amener le signal de fréquence intermédiaire à la portée basique. Pour les portées plus larges DDC doit être installé sur FPGA en combinant ainsi la flexibilité du but général DSP avec la grande vitesse et le petit prix de l'installation ASIC. On a présenté les mesurages et les computations pour les signaux d'entrée à cinq canaux en parallèle des deux dispositifs de FPGA. Dans ce papier on a considéré et discuté les avantages de grandes vitesses de la computation parallèle avec la présentation des performances du système et des résultats obtenus.

Mots clés: **radiogoniomètre, dispositif large bande, dispositif programmable, conversion des signaux.**